IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 13. (Cancelled)

14. (New) A multilayer wiring board having through holes in a thickness-wise direction,

wherein a semiconductor substrate mounted on the multilayer wiring board has through holes in a thickness-wise direction thereof, and wherein the through holes in the semiconductor substrate are located relative to the through holes in the multilayer wiring board so that entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas, which the through holes in the multilayer wiring board occupy.

15. (New) A multilayer wiring board having through holes in a thickness-wise direction,

wherein a semiconductor substrate mounted on the multilayer wiring board has through holes in a thickness-wise direction thereof, and wherein the through holes in the semiconductor substrate are located relative to the through holes in the multilayer wiring board so that entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise

direction of the multilayer wiring board and of the semiconductor substrate partly overlap areas which the through holes in the multilayer wiring board occupy.

16. (New) A multilayer wiring board having a cross-plane through hole or holes,

wherein an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is inside of a through hole or an area where through holes are built in the multilayer wiring board .

17. (New) A multilayer wiring board having through holes in a thickness-wise direction,

wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board.

18. (New) The multilayer wiring board according to one of claims 14 to 16, wherein conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

19. (New) The multilayer wiring board according to one of claims 14 to 16, wherein a semiconductor element is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

20. (New) The multilayer wiring board according to claim 14, wherein wirings, which connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

21. (New) A multilayer wiring board having cross-plane through holes,

wherein in-plane distribution of heat dissipated from a transistor or transistors of a semiconductor substrate mounted on the multilayer wiring board substantially coincides with distribution of the through holes.

22. (New) A multilayer wiring board having cross-plane through holes,

wherein in-plane distribution of heat dissipating from a transistor or transistors of a semiconductor substrate mounted on the multilayer wiring board substantially coincides with in-plane distribution of large and small cross-sections areas of the through holes.

23. (New) A wiring board,

wherein a semiconductor substrate having cross-plane through holes, which are connected to emitter wirings connected to emitters of heterojunction bipolar transistors and extended through the semiconductor substrate and which have conductive layers on sides thereof or inside thereof, is mounted on the multilayer wiring board, and the cross-plane through holes in the semiconductor substrate and through holes extending through the wiring board are connected to each other, and wherein conductive layers are provided on sides of or inside of the connected through holes in the semiconductor substrate and the wiring board, and in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board and of the semiconductor substrate are included in areas which the through holes in the multilayer wiring board occupy.

24. (New) A semiconductor device including a plurality of finger-shaped emitter electrodes or source electrodes, and at least one via hole which are arranged in rows in a first direction on a semiconductor substrate,

wherein the emitter electrodes or the source electrodes are connected to a conductive layer formed on a back surface opposite to a surface, on which the electrodes are formed, through the via hole, and

wherein said rows comprising the emitter electrodes or source electrodes, and the via holes are arranged in parallel in a second direction orthogonal to the first direction, and the via holes are positionally shifted from one another in adjacent rows among said rows, or adjacent rows are positionally shifted from one another in the first direction.

25. (New) The semiconductor device according to claim 24, wherein a multilayer wiring board has through holes formed on sides thereof or inside thereof, with a conductive layer, and areas, which the via holes of the semiconductor device occupies, overlap areas which the through holes of the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board.

Amendments to the Drawings:

The attached sheets of drawings includes changes to Figs. 9 and 10. These sheets, which includes Figs. 9 and 10, replaces the original sheet including Figs. 9 and 10. In Fig. 9, previously omitted element 7 has been added. In Fig. 10, corrections have been made regarding numerals 10A, 10B and 16 and 17.